A High Level Language Implementation of a General Purpose Telemetry System for Biomedical Applications

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Abstract

This paper describes a general purpose biomedical telemetry system consisting of an implantable VLSI chip and an RS232 compatible remote telemetry receiver. The implant supports a variety of programmable options to provide compatibility with a number of commercially available sensors. Additional hardware is included for the variation of sample rates and their occurrence to allow support for sensors of various speed. Also included is the capability to store samples in an internal static RAM, allowing the biological host to operate in its own environment without the need for an external monitor. Covered is the architecture of the proposed telemetry system, methods of implementation through HDL and comparative results obtained from these implementations.

1. Introduction

In the area of orthopaedic research, there is a lack of long term data on the structural integrity of artificial implants such as total joint systems. In addition, there exists a need for the continuous real-time monitoring of patients with devices such as fracture fixation plates and intramedullary rods to determine the healing rate. Obtaining necessary data presents considerable problems for the medical researcher due to the limited area in a biological host.[1]

Recently, advances in VLSI technology have made the design of self-contained telemetry devices much smaller and cost effective. These devices can be implanted in a test subject, transmitting data in real time without the need for external connection through biological tissue.

2. Objectives

The purpose of this project is to design and fabricate a monolithic microminiature implantable data acquisition and telemetry system for use with a variety of sensors. Implementation will be through VLSI, encompassing high-level design techniques and rapid prototyping during the development stage. The end product must be commercially viable and easily operated by a medical research team.

The project also involves refinement of fabrication techniques by which miniaturized electronic sensors are fabricated directly onto the surface of the orthopaedic implant for subsequent connection to the previously mentioned telemetry device. [1]

3. Specifications

The telemetry system consists of two main sections; the Biological Implant and the Remote Monitoring Unit (RMU). An implant consists of a VLSI die, power supply, and associated sensors to form the data acquisition portion of the telemetry system (Figure 1). Its primary function is to gather information inside a biological host and transmit it to the remote monitoring unit at a preprogrammed time. In order to perform this properly, the device needs to be flexible enough to support the specific need of the average biological sensor while being customized enough to exploit the full range of the device. This flexibility is achieved through the addition of programmability to the implant.

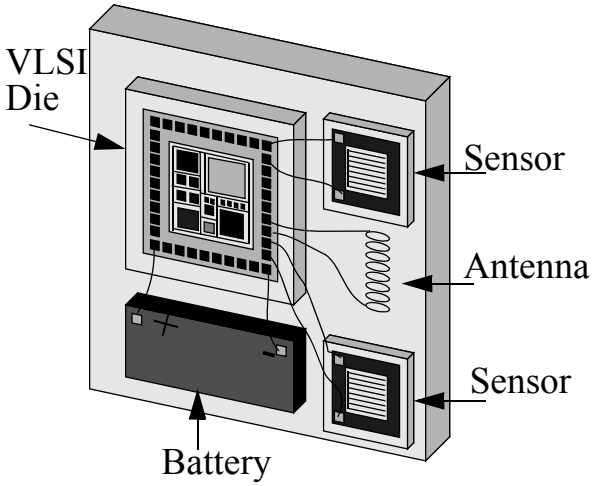

Figure 1. Implant environment

The remote monitoring unit encompasses a custom external communications transceiver connected to a host workstation. The RMU is burdened with the task of receiving, processing and storing the telemetry information from the implant. Data is received by the transceiver and transmitted to the host via either a serial or Enhanced Communications Port. Data is then captured by software executing on the host, allowing a number of operations to be performed. Key functions such as storage, signal

processing, and data visualization are accomplished on the host. Additionally, this software must be capable of creating the instruction sequences to program the implant. These instructions will define the number, speed and occurrence of the samples within the implant.

3.1 Application

The initial application involves measurement of orthopaedic implant stress using strain gage sensors. These sensors will be fabricated through laser ablation, forming the device directly on the surface of a fracture fixation plate. Similar sensor fabrication techniques can be utilized, however, to construct a variety of implant surface ion probes for measuring ph or electrolytes such as sodium, calcium, potassium, and magnesium which are intimately involved with bone mineral and/or osteoblast metabolism.[1]

3.2 Practical considerations

In order for these instrumented components to be acceptable from a medical perspective, the additional surface mounted instrumentation and biotelemetry systems must be unobtrusive, biocompatible, and in no way affect the established biomechanical performance of the surgical implant. It is these criteria that provide the greatest challenge for the designer.

Size constraints are based upon the area of the host for which the telemetry device is targeted. Applications involving relatively large medical implants, such as fracture fixation plates, contain a reasonably large flat surface for the location of components. Other devices, such as intramedullary rods, have difficult geometries requiring careful placement of the components in order to fit the entire system into a package.

In both of these cases the limiting factor is the size and placement of the power supply. For the purposes of this paper assumptions are made as to the availability of a reasonably priced, self-contained power source. For most applications these assumptions are valid due to the existence of polymer batteries in various geometries

The self-contained nature of the implant places constraints on the amount of space that the system can occupy. Since it can be assumed that the power supply is the size limiting factor, it would follow that power consumption would be the key in determining its size. It is for this reason that power conservation would be the most important design criterion. A CMOS design technology is necessary due to its low static and dynamic power dissipation. Additional logic is necessary to isolate the analog portions of the circuit during non-critical periods to reduce quiescent power drain.

In addition to size constraints, voltaic cells also have a limited lifetime. For long term studies, it may not be possible to use a cell that will remain charged for the life of the patient, even if its volt-hour capacity is not exceeded. Some method of guaranteeing power after a period of time or a battery failure must exist. For this reason, the addition of recharge circuitry is of great importance. This circuitry would allow batteries that have been used repeatedly or have degraded after long periods of inactivity to be revitalized to point where proper operation of the telemetry system is possible.

4. Digital controller

The digital controller consists of four main partitions: Control Logic, Communications Interface, Sample Timing & Interface, and the Memory Controller. This partitioned approach reduces complexity in two ways. First, since the burden of processing is distributed, the resulting sequential control logic is reduced to multiple smaller units as opposed to one large state machine. Hence, debugging is greatly simplified in the prototyping stage.

Additionally, the partitioned approach prevents modifications in one section of the hardware from effecting another section directly. For example, future modifications to the instruction decode logic would have minimal impact on the sample timing apparatus.

4.1 Control logic

The control logic is based around a micro-controller type architecture. Actions are performed based on the decoding of discrete instructions. This allows a modular approach to the design, resulting in a controller architecture that is easy to expand. It also reduces the size of the decode logic since the format is prearranged to make optimal use of the given command space.

4.2 Commands

Figure 2 shows the format for the command word. The word is arranged as two bytes, received least significant byte first. The most significant bit of each byte designates the current data being received.

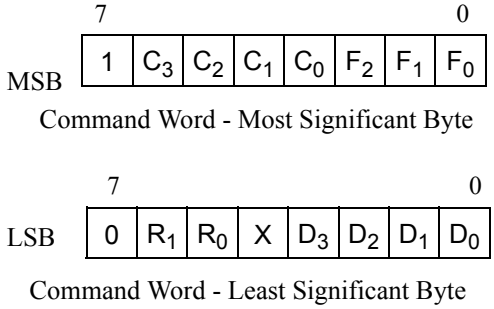

Figure 2. Command word format

This is important in performing resynchronization following the receipt of corrupted data. C_3-C_0 is the instruction nibble. It decodes to one of the 15 commands shown in Table 1

TABLE 1. Implant commands

C_3-C_0	Command
0000	Load Register
0001	Off-line
0010	On-line
0011	Echo
0100	Ping Toggle
0101	Power Down
0110	Power Up
0111	Real Time
1000	Transmit Status
1001	Enter Test Mode
1010	Reset
1011	Perform One Sample
1100	Read Memory Word
1101	Resend Memory Word
1110	Initialize Memory Address Reg.
1111	N/A

4.3 Power conservation logic

Of chief importance in the long term operation of the implant is the power conservation logic. This circuitry consists of transmission gates and other peripheral logic placed throughout the circuit to control the flow of current. When the controller decodes a power down instruction, all biasing current to the sensor subsystem and the transmitter portion of the RF transceiver is removed. The auxiliary power connection on the sensor interface is also disconnected.

Additionally, the clocks for the digital portion of the sensor interface are disabled. Since the static power drain of CMOS is extremely small, these sections can be left powered to retain the contents of the sequential memories. The control logic, communications interface logic, and RF receiver are the only functioning sections on the implant after power down.

With the implant in power down mode the battery drain is minimal. Also, battery charging operations can be enacted in the current state with little possibility of implant damage. Power down mode will continue until a corresponding power up command is decoded by the controller. At that point biasing current is restored to the analog portions and the clocks are reenabled. After a short stabilization period, the implant will return to normal operation.

4.4 Transmission verification logic

Transmission errors present in traditional wireless communications can be destructive to the experimental process. Telemetry devices can inadvertently receive commands that could eradicate previously stored data. To reduce the possibility of erroneous commands being accepted by the implant, Transmission Verification Logic (TVL) has been incorporated. This section works to reduce the number of errors received by adding redundant check data to transmissions.

The Transmission Verification Logic takes the incoming parallel data and performs arithmetic operations on it to determine the validity of the transmission. Only when determined to be an authentic transmission will the data be relayed to the controller logic. The verification process is accomplished through the use of information redundancy. The data is transmitted using a technique known as retransmission with complementation. Each byte of data destined for the implant in the remote monitoring unit is complemented and transmitted with the original to form a word. This word is subsequently received in the ART. The TVL then compares the data and signals the control logic when the verification is successful.

The TVL is also required to transmit signals to the RMU acknowledging the data transmissions. This procedure, known as handshaking, establishes a reliable link between the RMU and controller. If the TVL receives invalid information from the RMU, it responds with a status word giving the current operating state of the implant. This data will be interpreted as an error by the RMU which will retransmit the data. The cycle will continue until a signal is received from the implant, confirming that a valid transmission has been received.

4.5 Sample & timing logic

The Sample and Timing Logic is the controller of the analog-to-digital converter and its associated analog multiplexer. It is programmed by the control logic to generate an enable and a select signal based on each individual channel's sampling rate.

Each sensor channel consists of a register that points to the desired sampling rate through a multiplexor as shown in

Figure 7. These resulting signals are routed through a 4 to 1 priority encoder giving the A/D CONVERT signal as an output.

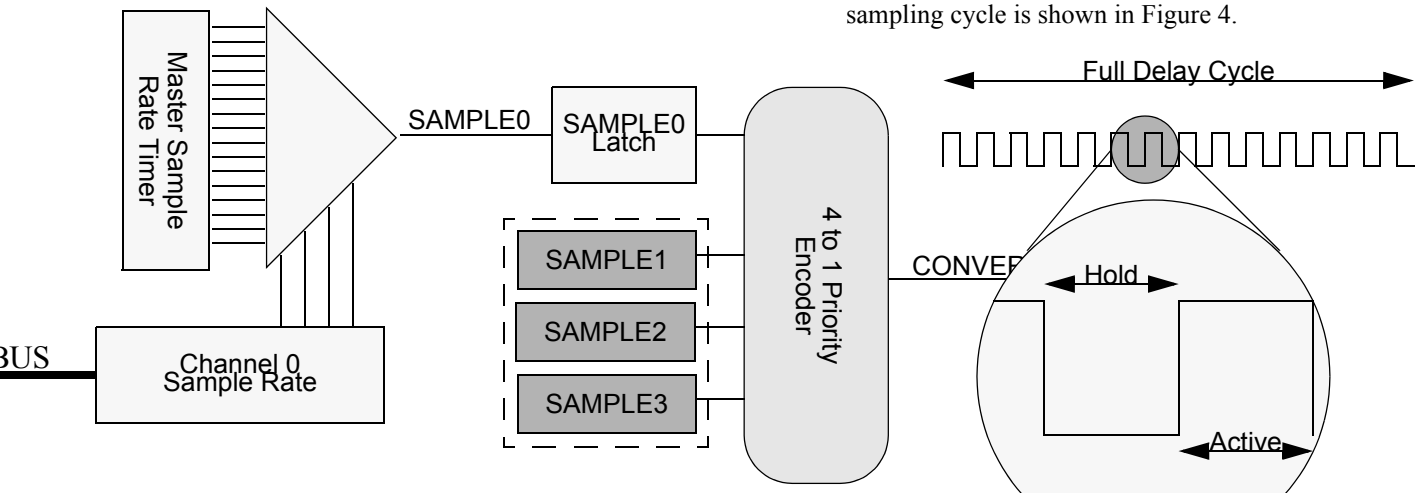

Figure 3. Sample rate determination logic

Contention is resolved by latching the outputs of each of the channels. If two channels attempt to sample simultaneously, the higher priority one will be processed first and the other will be held in the latch. After the first sample is completed, the second, still asserted, will be processed, assuming another higher priory channel does not generate a request first.

4.6 Delayed sampling

Additional logic is present in the interface to implement a delayed sampling operation. This delay cycle can be introduced in the sampling rate that will allow data capture at equal periods throughout the subject's daily cycle. The sampling cycle is shown in Figure 4.

Figure 4. Delayed sampling cycle

The sample start and stop registers define an enable signal with a duty cycle related to the contents of these registers. This signal can delay sampling for a period of up to 18 hours by selecting the most significant bit of the master counter. This can allow fast sampling sensors operating at 32KHz to take multiple samples over a long period and not exhaust the on board memory.

5. Digital controller layout

The first design for the digital controller was based on a rapid prototyping approach. This involved digital design through schematic capture under Powerview. The intended target would be a programmable logic device allowing a prototype to be quickly implemented. Once the prototype stage was reached, the decision to attempt layout via

structural netlist was obvious. This was accomplished by transferring the EDIF netlist to Epoch for technology targeting and layout. The process used was the Hewlett Packard 0.8 um, resulting in a design measuring 2500 x 2500 um^2.[2] Although the time involved was less than six months, the final layout was not cost effective.

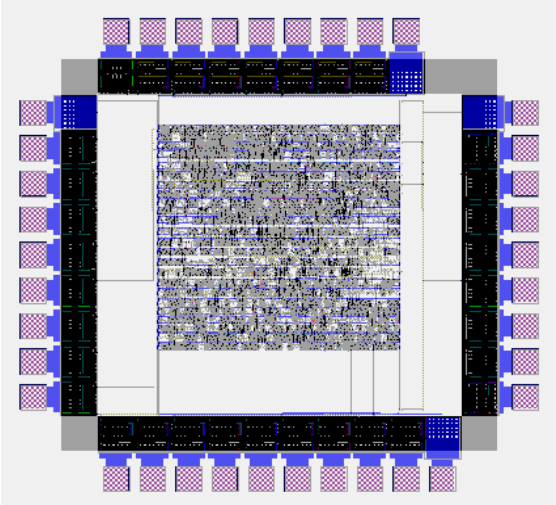

Figure 5. Standard cell layout

5.1 Second design - Physical level

This design consisted of an implementation of a reduced function digital controller with a limited sampling range. Layout involved logic design and simulation on Powerview to verify functional behavior, with subsequent standard cell and subsystem cell design and simulation using Magic. The top-down procedure involved cell placement design and floorplanning using a cell placement tool with subsequent global routing being performed by hand. All cells were built with cascadability in mind.

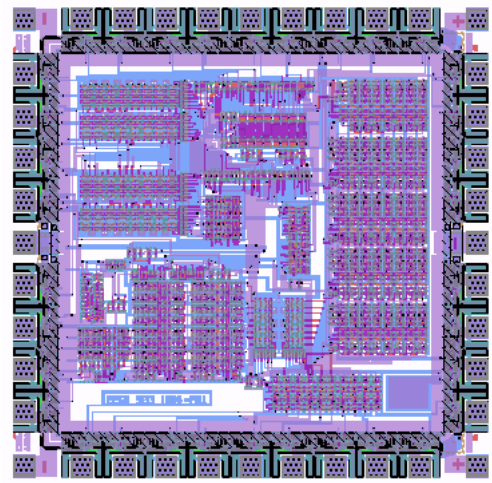

Figure 6. Magic layout

To minimize the total RC delay and the routing space, a cell placement algorithm (based on Simulated Annealing) was applied to the circuit model to find a local optimal solution for minimizing the lengths of the interconnections between the cells. The total area for the design is 2200x2200 um^2 under the Orbit 2 um fabrication process. The resulting chip is shown in Figure 6. [3]

5.2 Final design - Structural and behavioral level

From experience gained in the previous layout, the choice to move back to a higher level of abstraction was made. This was combined with a new design specification tool which allowed the use of MSI cells in a netlist.

The actual design was performed with a combination of structural VHDL and behavioral synthesis. This hybrid approach minimized the resulting design size by careful limitation of the amount of synthesis throughout the design. MSI logic was instantiated through Epoch structural netlists allowing a datapath cell layout. Synopsys behavioral synthesis was used for the finite state machines reducing the implementation time normally associated with complex next state logic.

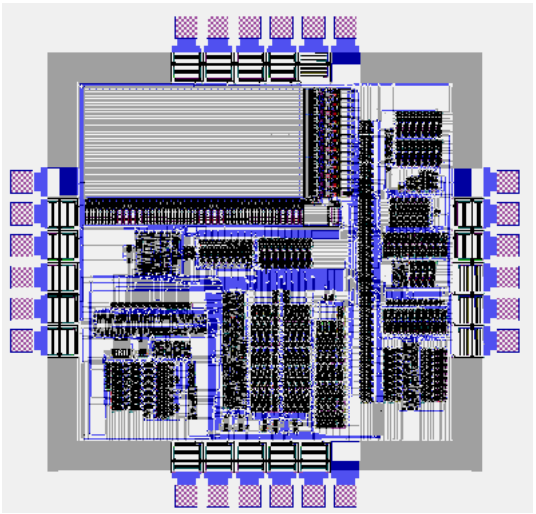

Figure 7. Automated layout

This approach resulted in a factor of 4 decrease in design to fabrication time relative to the physical approach. The resulting chip incorporates a controller with additional functionality. Included in the new design were the UART, 256 bytes of SRAM, feedback logic, TVL and an extended command set. The design also had a 50% reduction in layout area, adjusting for the change in fabrication processes. Total area for the design is 2500x2500 um^2 fabricated under the Hewlett Packard 0.8 um process (see Figure 7).