A Telemetric Instrumentation System for Orthopaedic Implants

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1.0 Introduction

Medical research is one of the most difficult experimental sciences that exist today. The difficulties in obtaining valid and useful data from a subject, without causing undue stress on the same, is both complex and expensive. The ultimate goal of medical experimentation is that of a reliable, safe method of monitoring complex biological functions in a way that would be transparent to the host.

The amount of data that can be obtained without the use of invasive procedures is limited, while the accuracy of data obtained through their use is subject to error. Additionally, invasive procedures present a real danger to the host. For this reason, many types of experimentation must be performed on test animals which provide a much less reliable method of study.

Recently, the advances in VLSI technology has made the design of self-contained telemetry devices much smaller and more cost effective. These devices can be implanted in a test subject, transmitting data in real time without the need for external connection through biological tissue. This type of monitoring is becoming more commonplace as researcher familiarize themselves with the new technology.

The basic purpose of this project is to design and fabricate a monolithic microminiature implantable data acquisition and telemetry system for use with orthopaedic devices such as fracture fixation plates, intramedullary rods, or total joint systems.   The project also involves refinement of fabrication techniques whereby miniaturized electronic sensors are fabricated directly onto the surface of the orthopaedic implant for subsequent connection to the previously-mentioned microprocessor system.

In order for these instrumented components to be acceptable from a medical perspective, the additional surface mounted instrumentation and biotelemetry system must be unobtrusive, biocompatible, and in no way affect the established biomechanical performance of the surgical implant. The initial application involves measurement of implant strains using strain gage sensors. Similar sensor fabrication techniques can be utilized, however, to construct a variety of implant surface ion probes for measuring ph or electrolytes such as sodium, calcium, potassium and magnesium which are intimately involved with bone mineral and/or osteoblast metabolism.

In 1966, Rydell [16] implanted an instrumented femoral head replacement for monitoring implant loading. Leadwires to foil strain gages within the implant neck were positioned subcutaneously and accessed by a small surgical incision six months post-operatively. A similar study recording strains on the prosthesis and on the femoral bone surface with sheep was conducted by Lanyon, et al. [14], in 1981.

Ongoing work, begun in 1974 by Carlson and Mann [6] and later by Rushfeldt and Mann [15] and Hodge, et al. [12,13] featured femoral heads instrumented with pressure transducers to monitor cartilage pressures at the joint. These devices also made use of radio telemetry for data transmission. Instrumented nail plates for the hip developed by Brown, et al. [4] and instrumented prosthesis by Brown, et al. [5] and Davy, et al. [8] first featured the use of semiconductor strain gages. In each of the femoral component applications, the gages were mounted to a hollowed-out surface in the interior of the implant.

Similar European efforts have been reported by Barlow, et al. [1], Bergmann, et al. [2]. Although there have been several examples of biotelemetry systems which have been designed to meet a relatively broad range of application [3,9,11,17], these systems have not been truly general purpose. The current project attempts to build on one recent effort to provide a comprehensive solution to the need for general purpose telemetry systems [7,10].

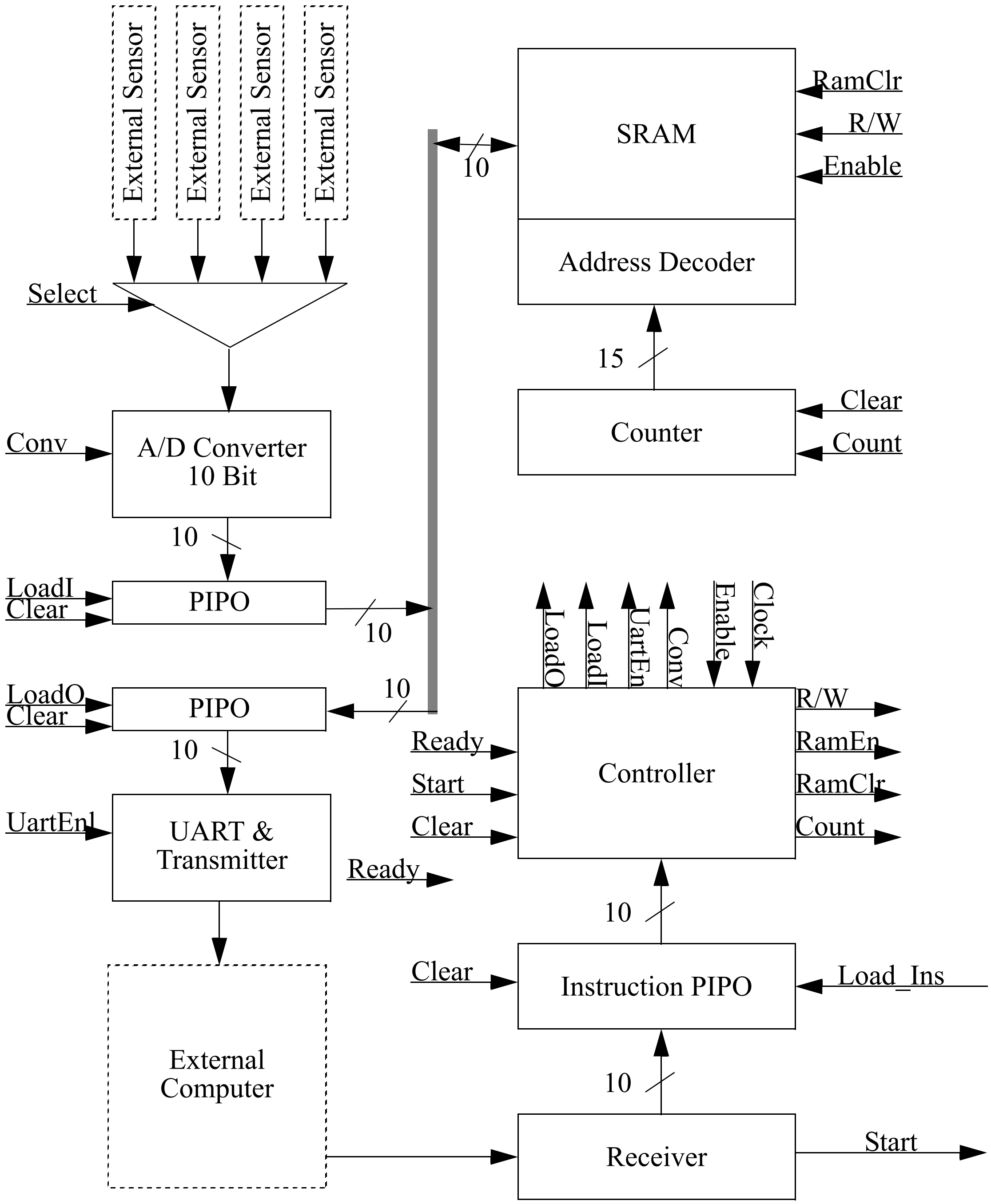
2.0 Data Acquisition System

The initial portion of this project has involved the design, simulation and fabrication of a monolithic telemetry controller with the following characteristics:

- Low Power Consumption
- Power-down Mode
- Programmable Sampling Rate
- Programmable Variable Sample Resolutions
- Programmable Sample Intervals
- On-Chip Data Storage

Figure X shows a schematic diagram of the entire data acquisition system.

FIGURE 1. Detailed Block Diagram of Biotelemetry Unit



2.1 System Command Register

The programming of the system is done via a 8-bit word, figure X, which is directly read from the UART (Universal Asynchronous Receiver Transmitter). When the UART has completely received 16 bits of data from the host computer, a valid signal will be enabled signifying that a valid word is available. This valid signal will stay asserted for one clock cycle. During this clock cycle, the system will decode the word and perform the functions outlined in figure 2.

FIGURE 2. Command Word Register

D_9	→								D_0	C_2	→	C_0	I_1	I_0	☒

TABLE 1. Command Instructions

C_2-C_0	Command
000	global reset
001	system interrupt
010	read memory
011	load sample duration registers
100	load the sample hold register
101	load the clock selection register
110	power off system
111	not used

- Global reset: This command overrides all operations within the system, except loading the clocks which will be discussed later. When this command is issued from the host computer, the system will be completely reinitialized, and will have to be reprogrammed. The following occurs upon receipt of the global reset command:
- All counters, registers and system controllers are reset.
- All stored data in the on-board RAM will be erased.

  The system will go into system interrupt mode.
- System interrupt: The system interrupt, or sample interrupt, puts the system into a state where samples are not taken regardless of how the system is programmed. Unlike the global reset, this command allows for the system to be put on hold for an indefinite amount of time without erasing anything. As already stated, the system is initially in the interrupt mode after being reset.

  If the system is in the interrupt mode and the interrupt command is issued, the system will move into sample mode.

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Whenever the interrupt command is issued and system is in interrupt mode, the mode of operation is determined by the value of I_1 in the command register. A low indicates direct transmission mode and a high indicates storage mode.

- Sample registers: These registers, one for each channel, hold the number of samples to be taken for each channel when taking measurements in the storage mode. D_9 through D_0 in the command register holds the value of the number of samples to be taken for each channel. I_1 and I_0 in the command register dictate which sample register receives the information stored in D_9 through D_0. When the *load sample register* command is issued, the data is loaded into the appropriate channel register.

  The number of samples to be taken is independent of the frequency at which they are taken.

- Sample hold register: This register is used to determine the amount of time for which the system will wait while taking measurements in the storage mode of sampling. D_9 through D_0 in the command register holds the value of the number of seconds for which the system will wait between taking sample sets. A sample set consists of all channels having taken all of their samples. When the *load sample hold register* command is issued, the data is loaded into the hold register.

  When samples are being taken in the storage mode, the system will initially wait for the amount time stored in the hold register. When this amount of time has expired, the system will then sample all channels for their respective amounts of samples and then hold again. At this point the cycle repeats itself.

- Clock register: When this command is issued, the system goes into a state where it will automatically load the clock register upon receipt of the next valid signal from the UART. Therefore, it takes two transmissions to successfully load the clocks into the system.

  There are sixteen clock frequencies available for which each channel can be sampled. In order to select between sixteen choices, a 4-bit word is need for each of the four channels which results in a 16-bit word that

2.2 Sample Frequencies

Below are the available clock frequencies for any of the four channels to be sampled at. The codes are loaded and stored in a 16-bit register, four bits for each channel.

TABLE 2. Clock Frequencies

Code	Frequency Hz.
0000	32768
0001	16384
0010	8192
0011	4096

TABLE 2. Clock Frequencies

Code	Frequency Hz.
0100	2028
0101	1024
0110	512
0111	256
1000	128
1001	64
1010	32
1011	16
1100	8
1101	4
1110	2
1111	1

2.3 Memory Controller

There is a need to temporarily store data in memory local to the implant controller for later transmission. This will allow the implant to sample data during a period of normal activity without running the risk of altering behavior to accommodate external storage devices. The memory controller will provide the necessary hardware to store and later recall sampled data.

The primary design goals of the memory controller are simplicity and independence of design. The design should occupy as little space on a final layout as possible. This reduces factors such as delay and power consumption. The design should also be as independent as possible so that any change to the memory controller or other sections of the implant will not require changes to the entire system.

2.3.1 Functional Description:

The memory controller stores data in a ram with a tag header that indicates the channel that is associated with the particular data element. A counter is used to determine the next available address. Once a sample is stored the counter will be incremented. Once all the data is stored and the implant is sent a request to transmit all stored data, the controller will decrement the counter and write the last data element. It continues decrementing the counter and writing data until all the data has been sent. A line from the decrementer will indicate that the last element has been reached. The data that is stored will be written to the controller in the opposite order that it was sampled.

The control and status lines that will be provided to the implant will be the read, write cs (chip select), write_busy, write_done, read_busy, read_done, r/w, and ram_enable. The control lines to the memory unit are the read, write, and cs lines. The read line starts the read for transmission process. The write line instructs the unit to store a sample. The cs line (chip select) must be asserted to tell the memory unit that the either the read line or write line has been asserted.

The status lines are write_busy, write_done, read_busy, and read_done. These lines tell the implant what the memory controller is currently doing. This is to insure that the controller will not be instructed to perform a new operation when an old one has not completed.

The remaining lines on the memory unit are used to control the static ram. These lines, the r/w and the ram_enable lines tell the SRAM what mode (read or write) to perform, and when to perform it (ram_enable). The address lines to the SRAM come from the output of the incrementing/decrementing counter. The data in lines come from the channel lines and the sampled data lines. The data out lines go directly to the transmitter.

2.3.2 Block Diagram:

The basic elements of the design include the controller, an incrementer/decrementer, and a parallel in/parallel out register. Also shown in the block diagram is the SRAM. Transmission gates are included with the SRAM to separate the data out and data in lines. Most commonly available SRAMS combine the data out/data in lines. The inc_dec line that goes from the controller to the incrementer/decrementer is used to tell which mode it should operate. If it is not asserted, the operation is increment, when it is asserted, decrementing is the mode of operation. The update_address line is the load line for the register. The overflow line that go from the incrementer/decrementer tells the controller that the last data element stored in the SRAM has been reached.

FIGURE 3.

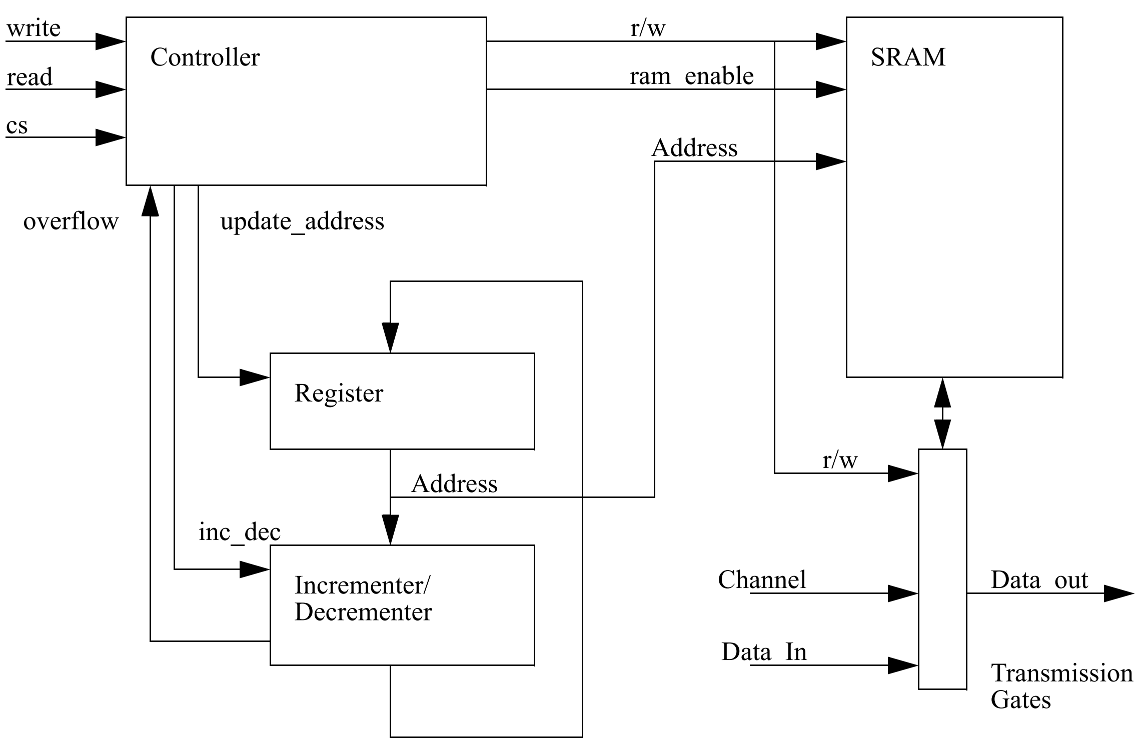
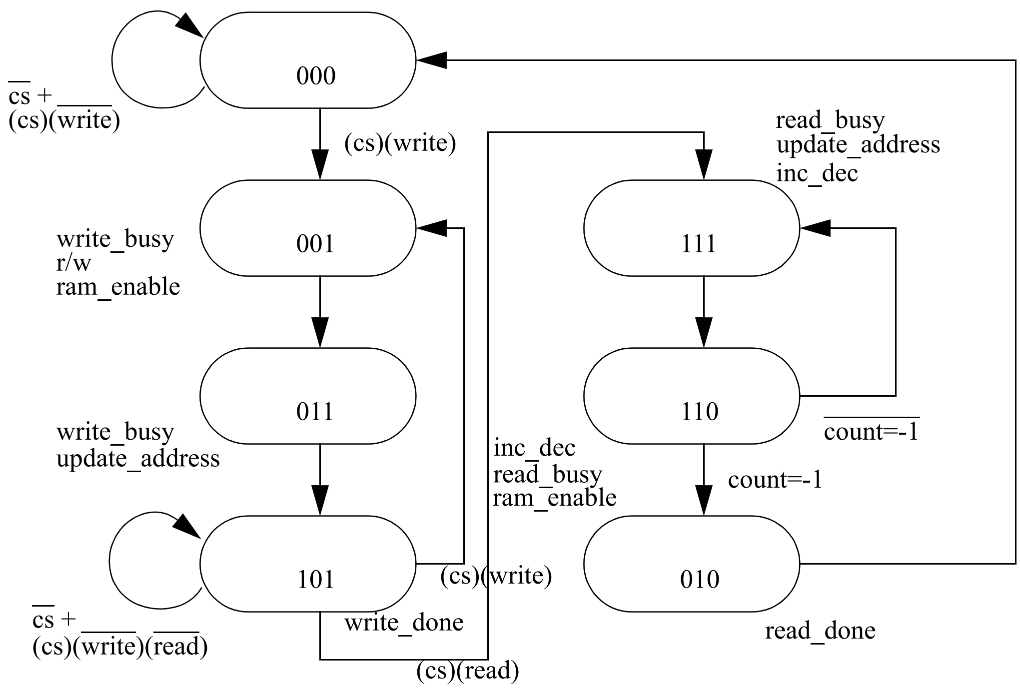


FIGURE 4.



2.3.3 Registers

Due to the limitations of FPGA's, special work must be done to accommodate a register. The FPGA does not give the designer control over the clock line to the flip-flops. All flip flops must share the same clock. A register will always load every clock cycle as a result. To overcome this problem, a multiplexer must be placed in the input of the flip-flops. When the load signal is unasserted, the multiplexer will tie the outputs of the flip-flops to the inputs. When the load signal is asserted, the multiplexer will tie the parallel load lines to the inputs of the flip-flops.

2.3.4 Incrementer / Decrementer

The incrementer / decrementer is implemented by using an adder, a multiplexer, and a register. The adder is fed the output of the register and the output of the multiplexer for it's inputs. The multiplexer will send the adder either a 1 or a -1 depending on whether the device is to increment or decrement. the register's load line accepts the count signal. The Incrementer / Decrementer contains the address of the next available memory location. The implementation of the incrementer/decrementer is shown below.

FIGURE 5. Command FSM

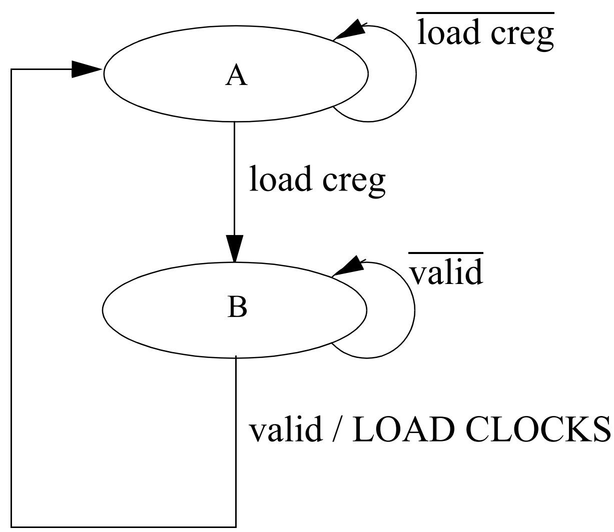


FIGURE 6. Sample and Delay FSM

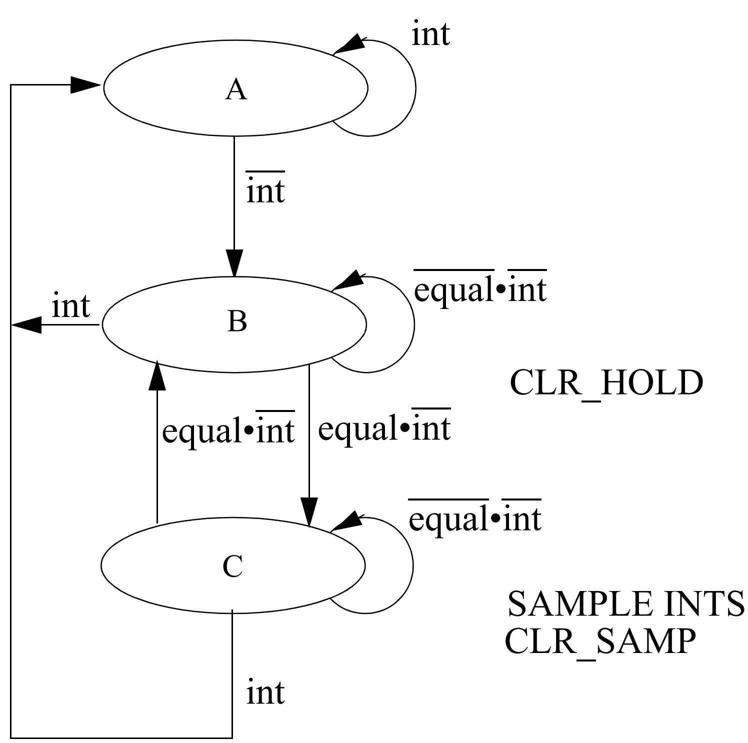


FIGURE 7. ADC Controller

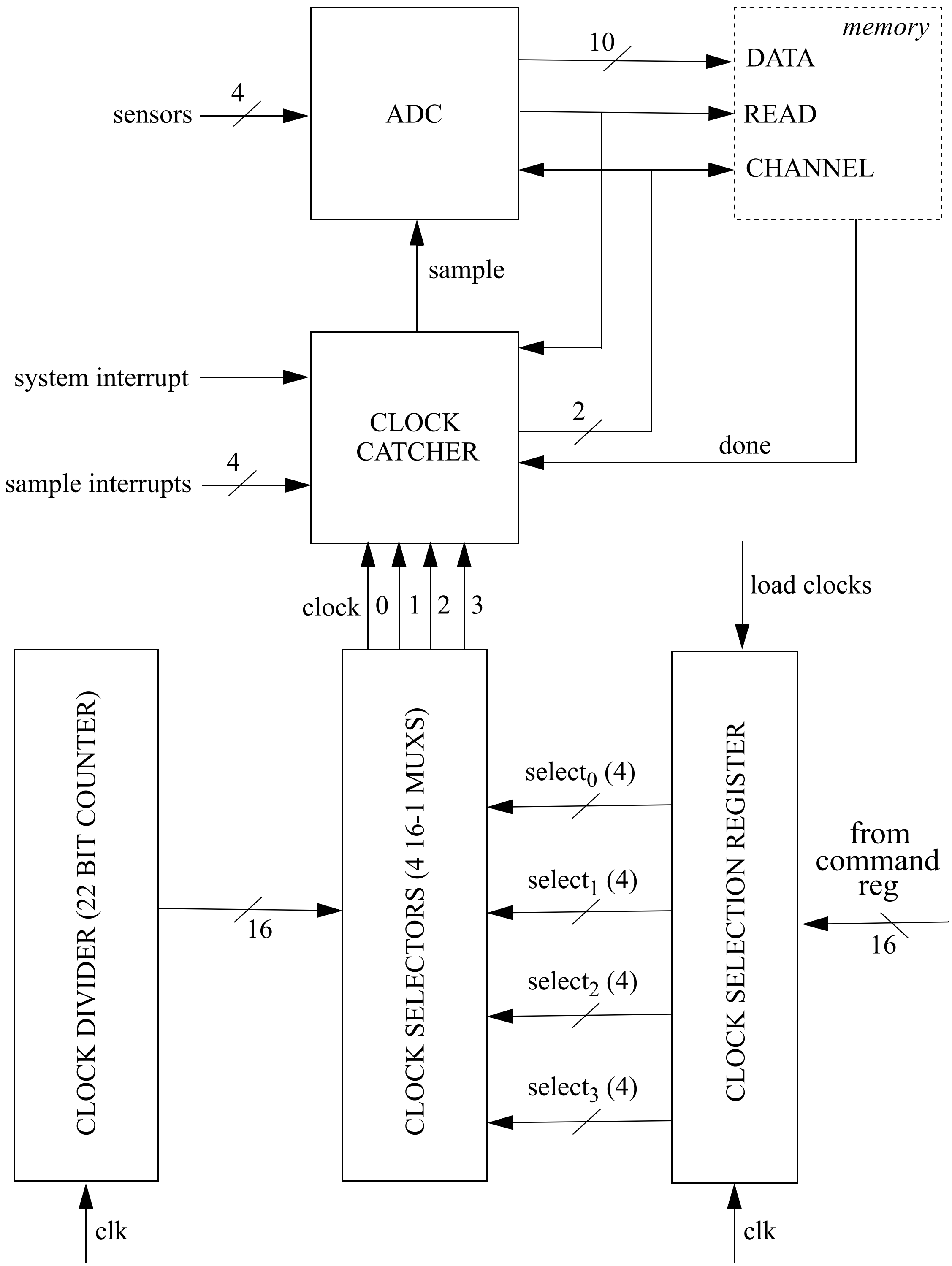
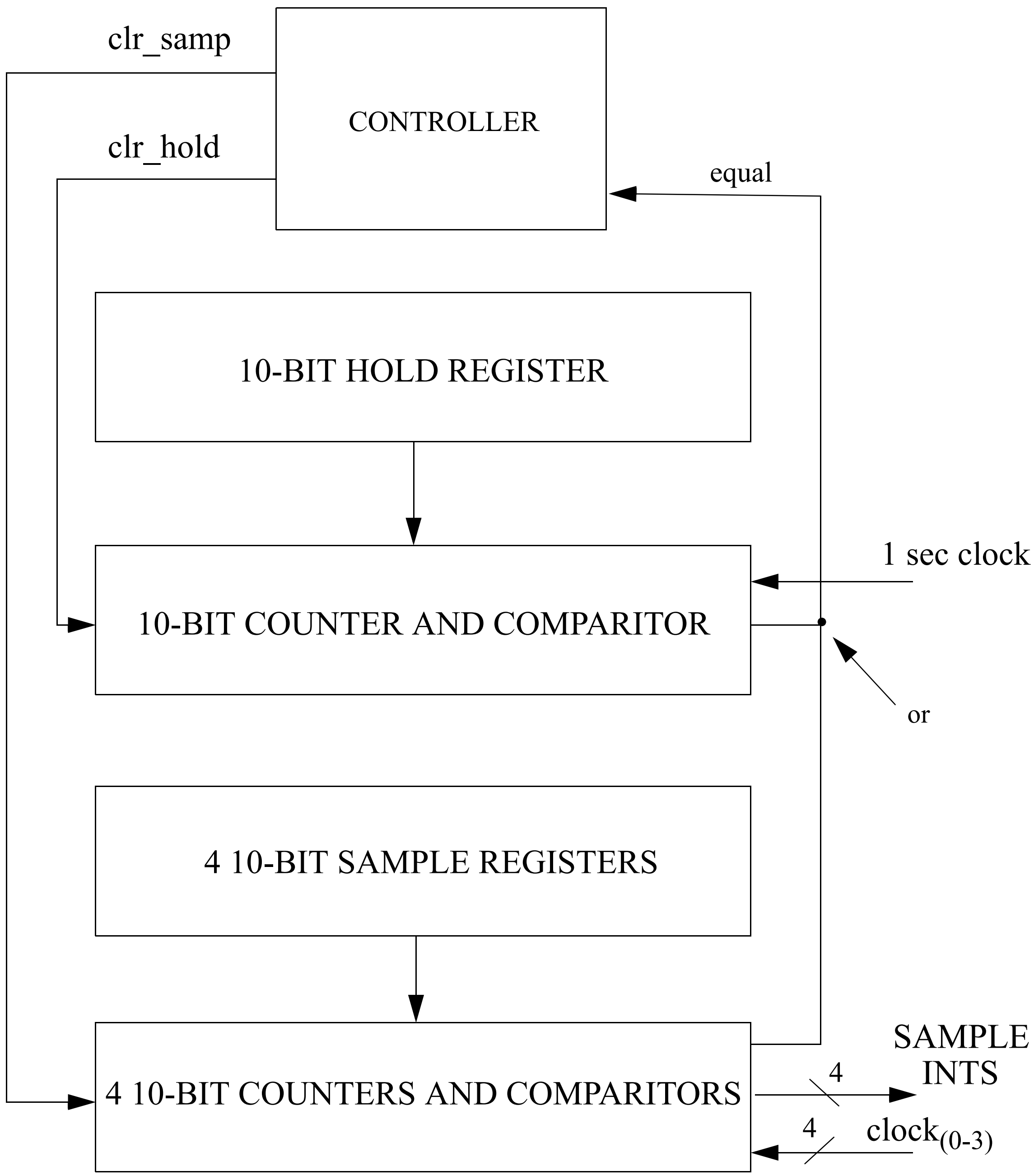


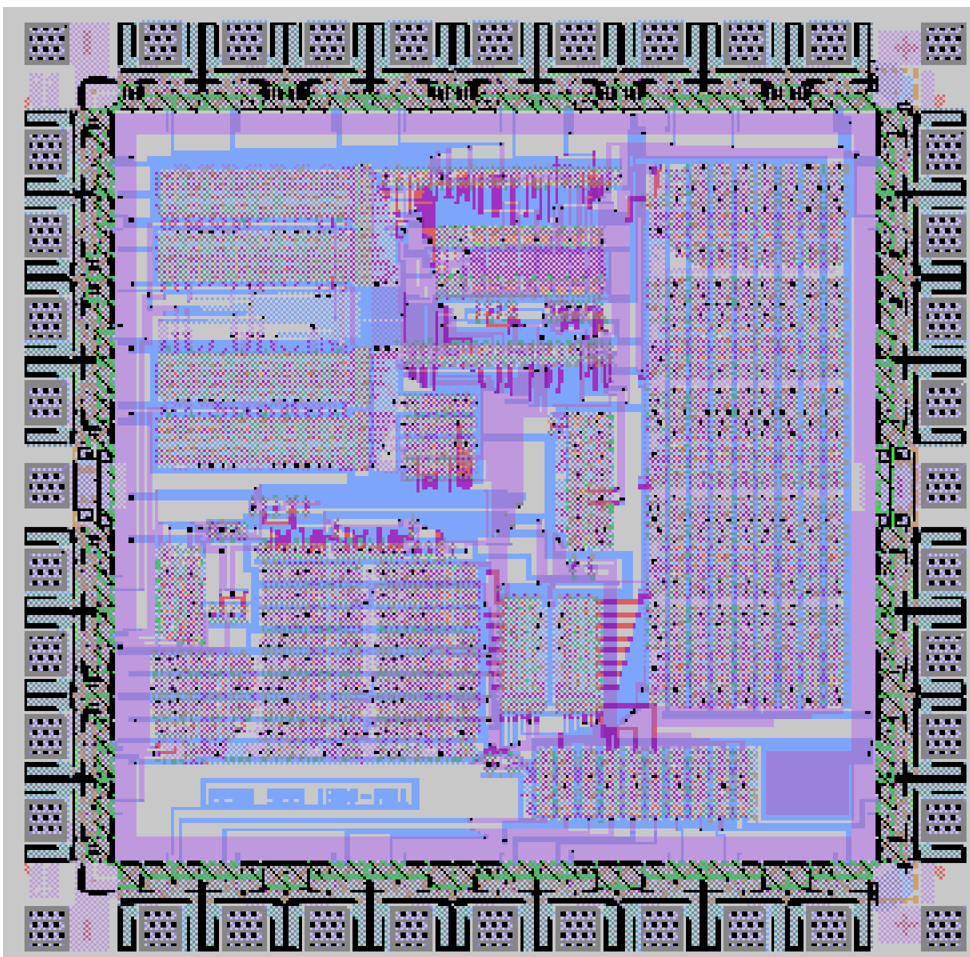
FIGURE 8. Sample and Delay Controller



3.0 Layout Considerations

A combination of bottom-up and top-down design approaches was followed, which helped to make the design layout more manageable. At the lowest level, all the basic standard cells were built and simulated. The bottom-up procedure involved logic design and simulation on Powerview, with subsequent standard cell and subsystem cell design and simulation using Magic. The top-down procedure involved cell placement design and floorplanning using a cell placement tool, Epoch, with subsequent global routing design and simulation. All cells were built with cascadability in mind. To minimize the total RC delay and the routing space, a cell placement algorithm (based on Simulated Annealing) was applied to the circuit model to find a global, optimal solution for minimizing the lengths of the interconnections between the cells. The total area for the design is 1600x1600 λ^2 (see Figure 3).

FIGURE 9. Magic Layout of Biotelemetry Chip



4.0 Sensor Fabrication

Typical implantable orthopaedic devices are primarily manufactured from titanium alloys, cobalt-chrome-molybdenum alloys or stainless steels. Sensor fabrication process development has been focused on the manufacture of strain gages in this project. The processes involved can be divided into three general areas: creation of an insulation layer, fabrication of the sensor and leadwire patterns, and the application of a biocompatible/protective thin film coating. Silicon oxide, chromium oxide and aluminum oxide thin films of 1 micron thickness have been evaluated as insulating layers subsequent to deposition on all of the previously listed implant materials. Aluminum oxide is most promising because it is not only a good insulator with good affinity for the sensor component materials but it has also shown promise as a bone ingrowth material (a bioactive glass). Fracture compression plates composed of 6Al4V-titanium have been primarily utilized for process development due to the moderate complexity of their design and the current popularity of the alloy.

Strain gages fabricated to this point consist of bismuth gages with surface dimensions of 50 x 750 microns with .5 micron thickness. Figure 4 shows a prototypical strain gage pattern of a bismuth gage on a silicon oxide thin film. The aluminum leadwire circuitry consists of lead paths 500 microns wide which traverse the compression plate for a length of 5.5 centimeters. Strain gages constructed of the stated materials for the stated dimensions exhibit a gage factor of approximately 50. Thermal evaporation deposition techniques were utilized for the bismuth and the aluminum films. Positive photoresist utilization after thin film deposition was found to be the most reliable method of circuit construction for the materials tested. A Shipley 1811 photoresist and a 422 developer were used for circuit pattern definition Aluminum leadwire paths are created first using a warmed PAE etchant. The bismuth gages are subsequently fabricated using a chromium etching solution which was found to rapidly etch bismuth without significantly affecting the previously deposited and etched aluminum. This design proved that long leadwires could be insulated from the base material and that mutilayer construction of the strain gages using dissimilar materials could be achieved. The integrated sensors have been mechanically tested in a half Wheatstone bridge configuration utilizing a passive resistor. Fatique tests to 10 million cycles have been conducted with no mechanical or electronic degradation of the integrated sensors.

Dificulties do exist, however, with using conventional photolithography techniques on complex 3-dimensional objects such as implantable orthopaedic devices. Currently tests are being conducted with regard to the utilization of laser ablation of the thin films to achieve circuit patterns on non-flat surfaces thus reducing or eliminating the need for photoresists and etchants.

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