VLSI Development of Smart-Pixel ICs: A Hybrid DSP Core and a Multi-threaded Programmable DSP

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Introduction:

Development of digital ICs with the capability to interface with optical devices to yield high-speed/high-bandwidth communication between chips has been underway. Presented here are two ICs which target this development. The first, fabricated with Hewlett-Packard's 14B half-micron process as a part of the 1997 Bell Labs/Lucent Technology CMOS-MQW foundry is a DSP core whose layout is shown in Figure 1. The second is a prototype design of the multi-threaded programmable DSP engine that will be a part of the 3-D OESP Consortium demonstrator system. The aim of the consortium is to develop dense packaging of DSPs with low power consumption and high-speed operation through use of free-space optical interconnect and realized with 3-D stacking of ICs.

DSP-Core Chip:

An early generation IC was designed to test and demonstrate the multiply-add structure that is common to many DSP algorithms. The DSP-core chip is a hybrid design which is compatible with both MQW modulators and VCSELs. One-hundred and twenty area-distributed I/O pads and eighteen perimeter pads provide electrical contacts for sixty MQW modulators which are flip-chip bonded to the surface of the die and eighteen VCSEL inputs. Analog receiver and driver arrays allow the digital core circuitry to communicate with these optical devices. Input to the chip can come optically via the modulators or electrically through perimeter pads. Both modulator and VCSEL driver outputs are active simultaneously. In addition, scan chains at the input and the output of the multiplier allow isolation of the hardware components as a test feature. The inputs are two 10-bit data words which are inputs to a 10x10 high-speed multiplier and a 20-bit data word which joins the multiplier output as the second input to an ALU. Perimeter pads also serve to control the ALU operation and provide clock and clear signals. To maintain signal integrity of the analog signals to and from the optical devices, receiver and driver arrays were placed as close as possible to the pads with which they communicate. Also, to reduce noise in the ground plane due to the digital circuitry switching, separate power and ground connections were included for the modulator receivers and for the VCSEL drivers.

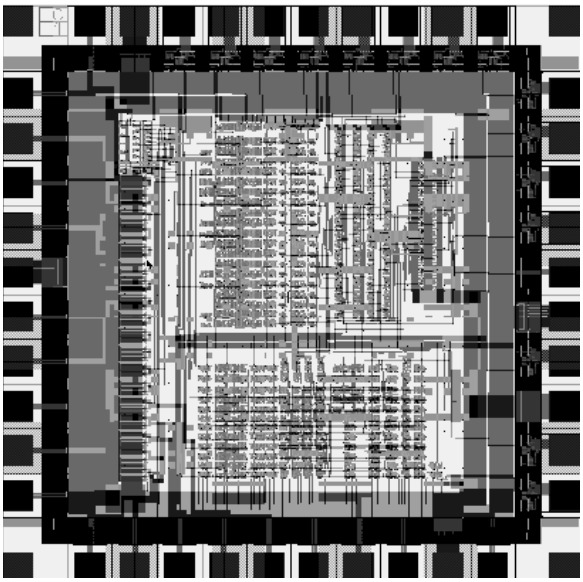

Figure 1: DSP-Core Chip layout

Multi-threaded Programmable DSP Chip:

The purpose of the second chip is to provide a prototype of the processor that will be a part of the multi-processor multi-chip 3-D OESP demonstrator system. This chip design extends upon the DSP core above to provide more flexibility and functionality.

The architecture for this chip, shown in Figure 2, is motivated by the desire to match the processor performance to the access time of the static RAM included with the processor. To achieve this, the separable nature of algorithms such as FFT and DCT was exploited. Multiple parts of the problem can be stored in separate RAMs and "threaded" through the processor so as to allow the RAM appropriate recovery time between accesses. The processor hardware

consists of four 24x12-bit multipliers and six add/subtract units. Precision through the processor is maintained by keeping all 36 bits from the multipliers and increasing the size of the add/subtract units in subsequent stages. The first two stages (multipliers and two adders) provide for complex multiplication. The third stage has programmable interconnect that allows for many different algorithms to be mapped into this hardware. Two of the four adder units in the third stage can be configured as accumulators which allows for complex multiply-accumulates to be performed.

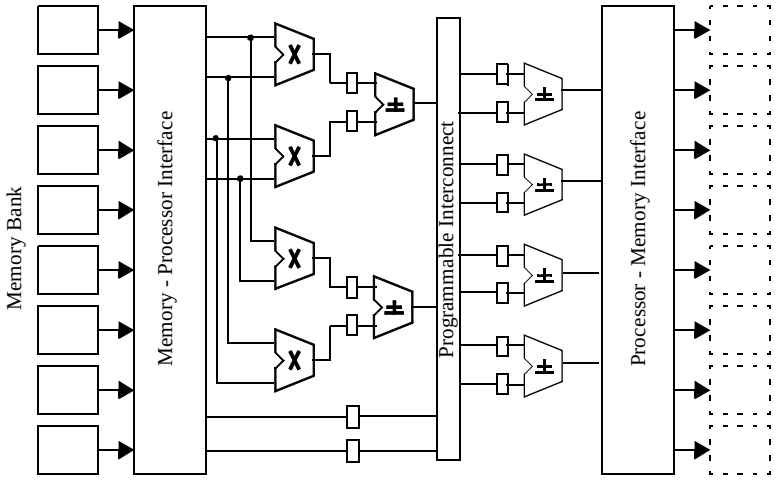

Figure 2: Prototype chip architecture

Eight separate SRAMs make up the memory bank. Only one bank of memory is included. The second memory bank shown in Figure 2 represents writing data back into the same bank from which it was taken. This RAM architecture was chosen based on the need to provide and receive two data points to and from the processor at each cycle in configurations such as the radix-2 butterfly and the need to have two clock cycles per RAM access.

Key to the high-performance operation of this design are the interface units between the processor and memory which provide data to the processor and write processed data back to memory with the appropriate timing. In general, data is taken from the RAMs four points at a time and stored in a register bank. Likewise another register bank stores data until it is written back to the RAMs four points at a time. This scheme allows the RAM to be accessed at every possible cycle (read or write) while maintaining the processor at full speed.

A bottleneck in current DSP systems lies in performing corner turns in two-dimensional calculations due to limited I/O bandwidth. The 3-D OESP demonstrator system will accelerate this process by allowing each of the 64 processors operating on the data in parallel to communicate with each other optically. A communication protocol and a system architecture based on this is also being developed [1]. To take advantage of the future high-bandwidth communication, large data ports will be will be supplied to send data out of each processor. Furthermore, four such processors will be on each IC in order to fill the 16x16 array of Giga-hertz optical channels. Therefore, the design of this chip also takes into consideration the need to operate the processors in parallel by minimizing the need to provide different control signals to different processors.

One of the goals of the prototype chip is to test the processor operation and develop state machines that will provide the best performance. For this reason, full external control of this chip is provided. In addition, scan chains allow for separate testing of the memory and processor. This prototype processor is going to be fabricated using Hewlett-Packard's 0.35µm-four metal-layer process. It has a total memory capacity of 49 kilo-bits and integrates just over half a million transistors. The die size is roughly 5x5 mm and will be packaged in a 108-pin PGA package.

Reference:

1. J. Rorie, P. Marchand, F. Kiamilev, P. Chandramani, J. Ekman, S. C. Esener, "A System Architecture for use with Free Space Optical Interconnects in a 3D Stacked Processor Environment".

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